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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,953	02/01/2000	Yoshiharu Kato	P8075-9034	4157

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	20

DATE MAILED: 01/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,953	KATO, YOSHIHARU	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *30-48* is/are withdrawn from consideration.

5)☒ Claim(s) *1-13,15 and 16* is/are allowed.

6)☒ Claim(s) *14 and 17-29* is/are rejected.

7)☒ Claim(s) *24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-29) in Paper No. 19 is acknowledged.

Claims 30-48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 19.

This application contains claims 30-48 drawn to an invention nonelected without traverse in Paper No. 19. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Arguments

2. Applicant's arguments with respect to claims 18-25, 28 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 24 and 25 are objected to because of the following informalities: -- judgment-- in the second to the last line of claims 24 and 25 is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 14 and 17-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "the second group of the bus lines" in line 3. The Examiner assumes the following was intended: a second group of the bus lines. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "the first group supplies" in line 5. The Examiner assumes the following was intended: the first group of first output circuits supplies. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "the second group supplies" in line 6. The Examiner assumes the following was intended: the second group of first output circuits supplies. There is insufficient antecedent basis for this limitation in the claim.

Claim 17 recites "one of the first logical output signal" which is incomprehensible. The Examiner assumes the following was intended: the first logical output signal.

Claim 18 recites the limitation "one of the bus lines" in line 4 (Note: it is not clear whether one of the bus lines refers back to one of the plurality of bus lines or another bus line). The Examiner assumes the following was intended: a bus line (Note: this change is required to give antecedent basis to "the bus line" in lines 6-7). There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites similar language as in claim 18, i.e., "one of the bus lines" in line 2.

Claim 21 recites the limitation "the first group supplies" in line 5. The Examiner assumes the following was intended: the first group of first output circuits supplies. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites the limitation "the second group supplies" in line 6. The Examiner assumes the following was intended: the second group of first output circuits supplies.

Claim 21 recites the limitation "the first output circuits" in line 2. The Examiner asserts that there is only one first output circuit in claim 18. There is insufficient antecedent basis for this limitation in the claim.

Claim 24 recites the limitation "the bus lines" in line 3. The Examiner assumes the following was intended: bus lines. There is insufficient antecedent basis for this limitation in the claim.

Claim 24 recites the limitation "each bus line" in line 4. The Examiner assumes the following was intended: a bus line. There is insufficient antecedent basis for this limitation in the claim.

Claim 25 recites the limitation "each bus line" in line 4. The Examiner assumes the following was intended: a bus line. There is insufficient antecedent basis for this limitation in the claim. Note it is not clear whether "each bus line refers back to the bus lines connecting the two semi-conductor devices or other buses within the semi-conductor devices since semi-conductor devices are replete with buses.

Claim 26 recites the limitation "the measuring semiconductor device" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 19-23, 28 and 29 depend from claim 18 hence inherit the deficiencies of claim 18.

Claim 27 depends from claim 26 hence inherit the deficiencies of claim 26.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 18, 22-25, 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama, Hideki (JP 05053857 A)

35 U.S.C. 102(b) rejection of claim 18.

Akiyama teaches an electronic device comprising first and second semiconductor devices connected (see LSI-A 10 and LSI-B 20 in Figure 1, Akiyama) to each other with a plurality of bus lines (see 103 and 104 in Figure 1, Akiyama), wherein the first semiconductor device includes (LSI-A 10 in Figure 1, Akiyama is a first semiconductor device): a first output circuit connected to a bus line for supplying the bus line with a first logical output signal (test circuit 6 in Figure 1, Akiyama is a first output circuit connected to a bus line 103 for supplying the bus line 103 with a first logical output signal), an inversion output circuit connected to bus lines for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the

first output circuit supplies the first logical output signal (inverter 1 in Figure 1, Akiyama is an inversion output circuit connected to bus lines 103, 104 and 105 for supplying the bus line 105 with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal), and a comparison circuit connected to a bus line (see comparator 5 in Figure 1, Akiyama); and the second semiconductor device (see LSI-B 20 in Figure 1, Akiyama) includes: an input circuit connected to a bus line for acquiring a first bus line signal (see test circuit 7 in Figure 1, Akiyama), and a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal (see test circuit 7 in Figure 1, Akiyama), wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device (see bus lines 107 & 108 and comparator 109, Akiyama).

35 U.S.C. 102(b) rejection of claims 22 and 23.

The Examiner would like to point out that test circuits 6 and 7 are the only output circuits for outputting data on lines 103 and 104 whether the data is test data or data generated under normal conditions (see Figure 1, Akiyama).

6. 35 U.S.C. 102(b) rejection of claim 24.

Akiyama teaches a first semiconductor (see LSI-A 10 and LSI-B 20 in Figure 1,

Akiyama) device that judges a connection between the first semiconductor device and a second semiconductor device (LSI-B 20 in Figure 1 in Akiyama is a second semiconductor device; Note: LSI-A 10 in Figure 1 in Akiyama comprises comparator 5 for judging a connection between the first semiconductor device and a second semiconductor device) connected thereto with bus lines, the first semiconductor device comprising: an output circuit connected to a bus line that supplies the bus line with a first logical output signal (test circuit 6 in Figure 1, Akiyama is a first output circuit connected to a bus line 103 for supplying the bus line 103 with a first logical output signal), wherein the second semiconductor device receives a first bus line signal and supplies a bus line with a second logical output signal being an inverted signal of the first bus line signal (LSI-B 20 in Figure 1 in Akiyama receives a first bus line signal on bus 103 and supplies bus line 105 via inverter 1 with a second logical output signal being an inverted signal of the first bus line signal); and a comparison circuit (see comparator 5 in Figure 1, Akiyama) connected to each bus line, that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device (see bus lines 107 & 108 and comparator 109, Akiyama).

7. 35 U.S.C. 102(b) rejection of claim 25.

a first semiconductor (see LSI-A 10 and LSI-B 20 in Figure 1, Akiyama) device that judges a connection between the first semiconductor device and a second

semiconductor device (LSI-B 20 in Figure 1 in Akiyama is a second semiconductor device; Note: LSI-A 10 in Figure 1 in Akiyama comprises comparator 5 for judging a connection between the first semiconductor device and a second semiconductor device) connected thereto with bus lines, the first semiconductor device comprising:

an output circuit connected to a bus line that supplies each bus line with a first logical output signal (test circuit 6 in Figure 1, Akiyama is a first output circuit connected to a bus line 103 for supplying the bus line 103 with a first logical output signal), wherein the second semiconductor device receives a first bus line signal (LSI-B 20 in Figure 1 in Akiyama receives a first bus line signal on bus 103);

an inversion output circuit connected to each bus line that supplies each bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplying the first logical output signal (inverter 1 in Figure 1, Akiyama is an inversion output circuit connected to bus lines 103, 104 and 105 for supplying the bus line 105 with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal); and

a comparison circuit connected to each bus line, that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgement signal regarding the connection between the first semiconductor device and the second semiconductor device (see bus lines 107 & 108 and comparator 109, Akiyama).

35 U.S.C. 102(b) rejection of claim 28.

The Examiner would like to point out that test circuits 6 and 7 in Figure 1 of Akiyama are inherently latch circuits for latching transmitted test data since digital data requires clocked sequential circuitry (or latches) to buffer incoming data prior to processing.

35 U.S.C. 102(b) rejection of claim 29.

See rejection to claims 26 and 28, above. In addition, test circuits 6 and 7 are connected to control lines 101, 102 and 111 (see Figure 1, Akiyama). Use of a reset signal for control would be an Engineering Design Choice, which does not deviate from the scope or the intent of the teachings in the Akiyama patent since Akiyama teaches control mechanisms for controlling test circuits 6 and 7, which encompass a particular embodiment such as a reset signal for controlling operation.

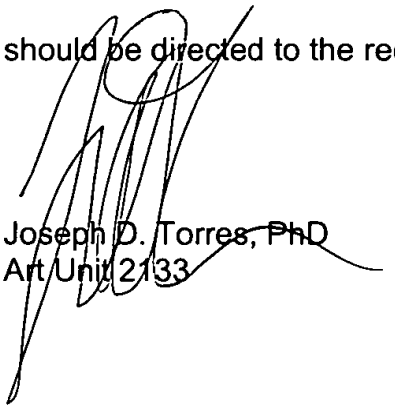
Allowable Subject Matter

8. Claims 1-13, 15 and 16 are allowed.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



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